Accordingly, Applicants respectfully request that the above-identified case be amended as follows prior to its further substantive consideration by the Examiner in this Request for Continued Examination proceeding:

IN THE CLAIMS:

Please amend the claims of this application so as to read as follows:

1. (Original) A shift register circuit, comprising:
a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;
a clock signal line transmitting a clock signal; and
a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein
potentials at nodes of the plurality of latch circuits vary in accordance with the pulse signal transferred;
the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits;
in at least a part of the period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency which is lower than in a normal operation period and which gradually increases; and
upon power-on, at least one of the switching circuits electrically disconnects at least one corresponding latch circuit from the clock signal line.

2. (Currently amended) A shift register circuit, comprising:
a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;
a clock signal line transmitting a clock signal; and
a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits according to control signals provided to said latch circuits, wherein
at least one of the switching circuits electrically disconnects at least one of the latch circuits from the clock signal line at power-on and at regular intervals thereafter in response to cyclic signals separate from said control signals.

D1 cont

3. (Original) The shift register circuit according to claim 2, wherein:
potentials at nodes of the plurality of latch circuits vary in accordance with the pulse signal transferred;
the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits; and
in at least a part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency lower than in a normal operation period.

4. (Canceled, without prejudice)

5. (Original) The shift register circuit according to claim 1, wherein the frequency of the clock signal in said at least a part of the period is from 1/2 to 1/16 of a frequency of the clock signal in a normal operation period.

6. (Original) The shift register circuit according to claim 2, wherein the frequency of the clock signal in said at least a part of the period is from 1/2 to 1/16 of a frequency of the clock signal in a normal operation period.

D1 cont

7. (Canceled, without prejudice)

8. (Original) The shift register circuit according to claim 1, wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and initializing an internal node of the latch circuit in response to the initialization signal.

9. (Currently Amended) ~~The~~ A shift register circuit ~~according to claim 2~~, comprising:

a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;

a clock signal line transmitting a clock signal; and

a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein

at least one of the switching circuits electrically disconnects at least one of the latch circuits from the clock signal line at regular intervals, and

wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and initializing an internal node of the latch circuit in response to the initialization signal.

D1 cont

10. (Original) The shift register circuit according to claim 1, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.

11. (Original) The shift register circuit according to claim 2, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.

12. (Original) The shift register according to claim 1, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.

13. (Original) The shift register according to claim 2, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.

14. (Original) The shift register circuit according to claim 1, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit further comprises a level shifter changing the amplitude of the clock signal received from outside.

P1 cont

15. (Original) The shift register circuit according to claim 2, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit further comprises a level shifter changing the amplitude of the clock signal received from outside.

16. (Original) An image display device of active matrix type, comprising:
a plurality of pixels arranged in a matrix form;
a data signal line supplying video data to be written to one of the plurality of pixels;
a scan signal line for controlling the writing of the video data to one of the plurality of pixels;
a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and
a scan driver supplying a pulse signal to the scan signal line in synchronization with a timing signal,
at least one of the data driver and the scan driver comprising the shift register circuit according to claim 1.

17. (Original) An image display device of active matrix type, comprising:
a plurality of pixels arranged in a matrix form;
a data signal line supplying video data to be written to one of the plurality of pixels;
a scan signal line for controlling the writing of the video data to one of the plurality of pixels;
a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and
a scan driver supplying a pulse signal to the scan signal line in synchronization with a timing signal,
at least one of the data driver and the scan driver comprising the shift register circuit according to claim 2.

D1 cnt

18. (Original) The image display device according to claim 16, wherein the data driver has the shift register circuit, and initializes the potential level at each of the internal nodes of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.

19. (Original) The image display device according to claim 17, wherein the data driver has the shift register circuit, and initializes the potential level at each of the internal nodes of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.

20. (Original) The image display deice according to claim 16, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels also are formed.

21. (Original) The image display deice according to claim 17, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels also are formed.

22. (Original) The image display device according to claim 20, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.

D1 cont

23. (Original) The image display device according to claim 20, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.

24. (Original) The image display device according to claim 22, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600° C or lower.

25. (Original) The image display device according to claim 23, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600° C or lower.

26-34. (Canceled, without prejudice)

35. (Previously presented) A shift register circuit, comprising:

a plurality of latch circuits connected in series to sequentially transfer a pulse signal from one to another;

a clock signal line transmitting a clock signal;

a plurality of switching circuits performing electrical connection and disconnection between the clock signal line and the plurality of latch circuits, wherein at least one of the switching circuits electrically disconnects at least one of the plurality of latch circuits from the clock signal line at regular intervals;

potentials at nodes of the plurality of latch circuits vary in accordance with the pulse transferred;

D1 cont

the plurality of switching circuits each connect or disconnect corresponding latch circuits to or from the clock signal line in accordance with the potentials at the nodes of the corresponding latch circuits; and

in at least part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has a frequency lower than in a normal operation period;

wherein the frequency of the clock signal gradually increases in at least part of said period.

36. (Previously presented) The shift register circuit according to Claim 35, wherein the

frequency of the clock signal in said at least a part of the period is from 1/ 2 to 1/16 of a frequency of the clock signal in the normal operation period.

37. (Previously presented) The shift register circuit according to Claim 35, wherein each latch circuit has an initialization circuit receiving an initialization signal from outside and initializing an internal node of the latch circuit in response to the initialization signal.

38. (Previously presented) The shift register circuit according to Claim 35, wherein the clock signal has an amplitude smaller than an amplitude of a power-supply voltage of the shift register circuit.

D1 cnt

39. (Previously presented) The shift register circuit according to Claim 35, further comprising a buffer circuit supplying the plurality of latch circuits with a clock signal received from outside.

40. (Previously presented) The shift register circuit according to Claim 35, wherein a clock signal received from outside has an amplitude different from an amplitude of the clock signal supplied to the plurality of latch circuits, and the shift register circuit further comprises a level shifter changing the amplitude of the clock signal received from outside.

41. (Previously presented) An image display device of active matrix type, comprising:

a plurality of pixels arranged in a matrix form;

a data signal line supplying video data to be written to one of the plurality of pixels;

a scan line for controlling the writing of the video data to one of the plurality of pixels;

a data driver supplying the video signal to the data signal line in synchronization with a timing signal; and

a scan driver supplying a pulse signal to the scan line in synchronization with a timing signal;

at least one of the data driver and the scan driver comprising the shift register circuit according to claim 35.

D1 cont

42. (Previously presented) The image display device according to claim 41, wherein the data driver has the shift register circuit, and initializes the potential level at each internal node of the plurality of latch circuits in the shift register circuit in synchronization with a vertical synchronous signal.

43. (Previously presented) The image display device according to claim 41, wherein at least one of the data driver and the scan driver is formed on a substrate on which the plurality of pixels are also formed.

44. (Previously presented) The image display device according to claim 43, wherein active devices included in at least the data driver comprise polysilicon thin-film transistors.

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45. (Previously presented)) The image display device according to claim 44, wherein the active devices have been formed on a glass substrate by a process at a temperature of 600° C or lower.